Amendments to the Specification

Please replace the Title with the following new Title:

Clock Synchronizer with Offset Prevention Function against Variation of Output Potential of Loop Filter

Please replace the paragraph beginning at page 23, line 33 with the following amended paragraph:

B'

In the conventional PLL circuit shown in Fig. 23, assuming that potential VC of node N122 [[N102]] is ground potential GND before the power-supply is turned on, and potential VC of node N122 [[N102]] in the locked state is VCC/2, current Ic flowing through P-channel MOS transistor 123 [[103]] supplies charge to node N122 [[N102]] for a period from the power-up until the locked state is reached. Current Ic at this moment is increased as potential VC of node N122 [[N102]] is lowered. Thus, in the conventional PLL circuit, while there is a disadvantage in that current Ic and Id disagree with each other generating an offset, there is an advantage in that the time period from the power-up to the locked state is short.